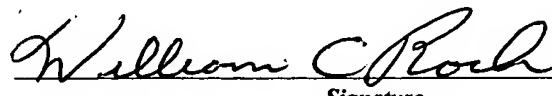
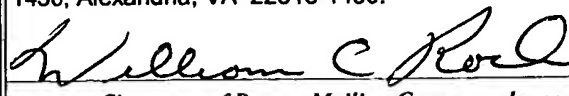


IFW

TRANSMITTAL OF FORMAL DRAWINGS			Docket No. BUR920040001US1 (17382)	
In Re Application Of: John M. Cohn, et al				
Serial No. 10/709,754	Filing Date May 26, 2004	Confirmation No. Unassigned	Examiner Unassigned	Art Unit Unassigned
Invention: FPGA ICE BREAKPOINT/LOGIC EC				
Address to: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450				
Transmitted herewith are: 2 sheets of formal drawing(s) for this application. <input checked="" type="checkbox"/> Each sheet of drawing indicates the identifying indicia suggested in 37 CFR Section 1.84(c).				
<div style="text-align: center;"> <i>Signature</i></div> <div style="border: 1px solid black; padding: 5px; margin-top: 10px;">William C. Roch, Esq. Registration No. 24,972</div>			Dated: <u>June 3, 2004</u>	
Correspondence Address Customer No.: 23389			<div style="border: 1px solid black; padding: 5px;"><small>I certify that this document and attached formal drawings are being deposited on 6/3/04 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</small></div> <div style="text-align: center; margin-top: 10px;"> <i>Signature of Person Mailing Correspondence</i></div> <div style="text-align: center; margin-top: 10px;">William C. Roch <i>Typed or Printed Name of Person Mailing Correspondence</i></div>	